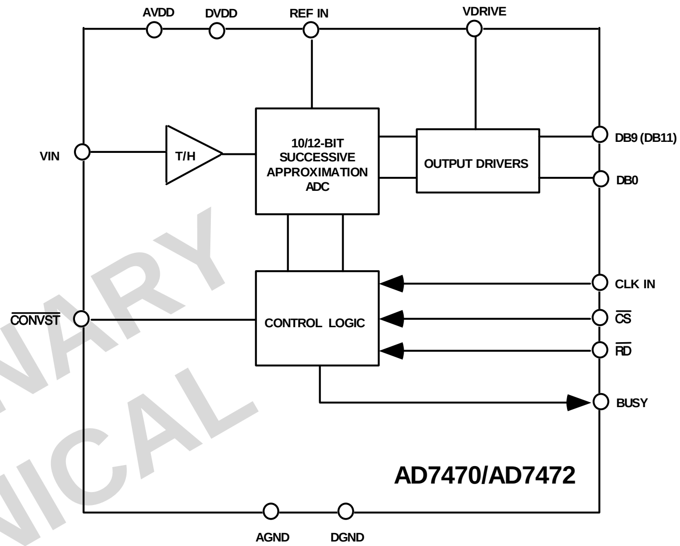
1.75MSPS, 4mW 10-Bit/12-Bit SAR ADC

Preliminary Technical Data

AD7470/72

FEATURES
Specified for V_{DD} of 2.7 V to 5.25 V
1.75MSPS for AD7470 (10-Bit)
1.5MSPS for AD7472 (12-Bit)
Low Power:
3mW typ at 1.75MSPS with 3V Supplies
9mW typ at 1.75MSPS with 5V Supplies
Wide Input Bandwidth:
70dB SNR at 500kHz Input Frequency
Flexible Power/Throughput Rate Management
No Pipeline Delays
High Speed Parallel Interface
Shut Down Mode: 500nA typ.
24-Pin SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



AD7470 is a 10 Bit part with DB0 to DB9 as outputs
AD7472 is a 12 Bit part with DB0 to DB11 as outputs

GENERAL DESCRIPTION

The AD7470/AD7472 are 10-bit /12-bit high speed, low power, successive-approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5MSPS for the 12-bit AD7472 and up to 1.75MSPS for the 10-bit AD7470. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 1MHz.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The BUSY goes high at the start of conversion and goes low 465ns later to indicate that the conversion is complete. There are no pipelined delays associated with the part. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7470/AD7472 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 3V supplies and 1.75MSPS throughput rate, the parts consume just 1mA. With 5V supplies and 1.75MSPS, the current consumption is 1.8mA. The part also offers flexible power/throughput rate management. Operating the part with 3V supplies and 500ksps throughput reduces the current consumption to 0.5mA. At 5V supplies and 500ksps, the part consumes 0.8mA.

It is also possible to operate the parts in an auto shutdown mode, where the part powers up to do a conversion and automatically enters shutdown mode at the end of conversion.

Using this method allows very low power dissipation numbers at lower throughput rates. In this mode, the parts can be operated with 3V supplies at 100ksps, and consume an average current of just 150uA. At 5V supplies and 100ksps, the average current consumption is 270uA.

The analog input range for the part is 0 to REF IN. The +2.5V reference is applied externally to the REF IN pin. The conversion rate is determined by the externally-applied clock.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption the AD7470 offers 1.75MSPS throughput and the AD7472 offers 1.5MSPS throughput rates with 3mW power consumption.
2. Flexible Power/Throughput Rate Management
   The conversion rate is determined by an externally-applied clock allowing the power to be reduced as the conversion rate is reduced. The part also features an autoshutdown mode to maximize power efficiency at lower throughput rates.
3. No Pipeline Delay.
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

REV. PrD 09/98

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AD7470–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK IN}$ = 28 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal to Noise + Distortion (SINAD)[2]	58	dB min	f_{IN} =500kHz Sine Wave, f_S = 1.75Msps
Signal to Noise Ratio (SNR)[2]	59	dB min	f_{IN} =500kHz Sine Wave, f_S = 1.75Msps
Total Harmonic Distortion (THD)	–70	dB max	f_{IN} =500kHz Sine Wave, f_S = 1.75Msps
Peak Harmonic or Spurious Noise (SFDR)	–70	dB max	f_{IN} =500kHz Sine Wave, f_S = 1.75Msps
Intermodulation Distortion (IMD)			
Second Order Terms	–75	dB typ	
Third Order Terms	–75	dB typ	
Aperture Delay	tbd	ns typ	
Aperture Jitter	tbd	ns typ	
Full Power Bandwidth	20	MHz typ	
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits.
Offset Error	±1	LSB max	
Gain Error	±1	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF IN	Volts	
dc Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF IN Input Voltage Range	2.5	V	+/-1% for Specified Performance
dc Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS	(Vdd=5) (Vdd=3)	Volts	
Input High Voltage, V_{INH}	2.8 2.4	V min	
Input Low Voltage, V_{INL}	0.4 0.4	V max	
Input Current, I_{IN}	±1 ±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10 10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200mA
Floating-State Leakage Current	±10	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	pF max	
Output Coding	Straight(Natural) Binary		
CONVERSION RATE			
Conversion Time	12	CLK IN cycles	428ns with CLK IN at 28MHz
Track/Hold Acquisition Time	100	ns max	
Throughput Rate	1.75	MSPS max	Conversion Time + Acquisition Time. CLK IN at 28MHz

AD7470—SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 28 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+2.7/+5.25	V min/max	
I_{DD}[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	2.2	mA max	Typically 1.8mA. V_{DD} = 4.75V to 5.25V. f_S=1.75MSPS
Normal Mode	1.33	mA max	Typically 1mA. V_{DD} = 2.7V to 3.3V. f_S=1.75MSPS
Shutdown Mode	1	µA max	CLK IN =0V or DV_{DD}
Power Dissipation[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	11	mW max	V_{DD} = 5V.
	4	mW max	V_{DD} = 3V
Shutdown Mode	5	uW max	V_{DD} = 5 V. CLK IN =0V or DV_{DD}
	3	µW max	V_{DD} = 3 V. CLK IN =0V or DV_{DD}

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3] Sample tested @ +25°C to ensure compliance.
[4] See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

AD7472–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 28 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal to Noise + Distortion (SINAD)[2]	69	dB min	f_{IN} =500kHz Sine Wave, f_S = 1.5Msps
Signal to Noise Ratio (SNR)[2]	70	dB min	f_{IN} =500kHz Sine Wave, f_S = 1.5Msps
Total Harmonic Distortion (THD)	–76	dB max	f_{IN} =500kHz Sine Wave, f_S = 1.5Msps
Peak Harmonic or Spurious Noise (SFDR)	–76	dB max	f_{IN} =500kHz Sine Wave, f_S = 1.5Msps
Intermodulation Distortion (IMD)			
Second Order Terms	–78	dB typ	
Third Order Terms	–78	dB typ	
Aperture Delay	tbd	ns typ	
Aperture Jitter	tbd	ns typ	
Full Power Bandwidth	20	MHz typ	
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits.
Offset Error	±3	LSB max	
Gain Error	±3	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF IN	Volts	
dc Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF IN Input Voltage Range	2.5	V	+/-1% for Specified Performance
dc Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
LOGIC INPUTS	(Vdd=5) (Vdd=3)	Volts	
Input High Voltage, V_{INH}	2.8 2.4	V min	
Input Low Voltage, V_{INL}	0.4 0.4	V max	
Input Current, I_{IN}	±1 ±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10 10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200mA
Floating-State Leakage Current	±10	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	pF max	
Output Coding	Straight(Natural) Binary		
CONVERSION RATE			
Conversion Time	14	CLK IN cycles	500ns with CLK IN at 28MHz
Track/Hold Acquisition Time	100	ns max	
Throughput Rate	1.5	MSPS max	Conversion Time + Acquisition Time. CLK IN at 28MHz

AD7472–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 28 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+2.7/+5.25	V min/max	
I_{DD}[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	2.2	mA max	Typically 1.8mA. V_{DD} = 4.75V to 5.25V. f_S=1.5MSPS
Normal Mode	1.33	mA max	Typically 1mA. V_{DD} = 2.7V to 3.3V. f_S=1.5MSPS
Shutdown Mode	1	uA max	CLK IN =0V or DV_{DD}
Power Dissipation[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	11	mW max	V_{DD} = 5V.
	4	mW max	V_{DD} = 3V
Shutdown Mode	5	uW max	V_{DD} = 5 V. CLK IN =0V or DV_{DD}
	3	uW max	V_{DD} = 3 V. CLK IN =0V or DV_{DD}

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3] Sample tested @ +25°C to ensure compliance.
[4] See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7470	AD7472	Units	Description
f_{CLK} [2]	1	1	kHz min	
	28	28	MHz max	
$t_{CONVERT}$	12* t_{CLK}	14* t_{CLK}		t_{CLK}= 1/$f_{CLK\ IN}$
	428	500	ns max	$f_{CLK\ IN}$ = 28MHz
t_{WAKEUP}	1	1	us max	Wakeup Time
t_{acq}	100	100	ns max	Acquisition Time
t_1	15	15	ns min	$\overline{CONVST}$ Pulse Width
t_2	10	10	ns min	$\overline{CONVST}$ to BUSY Delay
t_3	0	0	ns max	BUSY to $\overline{CS}$ Setup Time
t_4 [3]	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	30	30	ns min	$\overline{RD}$ Pulse Width
t_6 [4]	25	25	ns min	Data Access Time After Falling Edge of $\overline{RD}$
t_7 [5]	5	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
t_8	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts. See Figure 2.

[2]Mark/Space ratio for the CLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_7 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

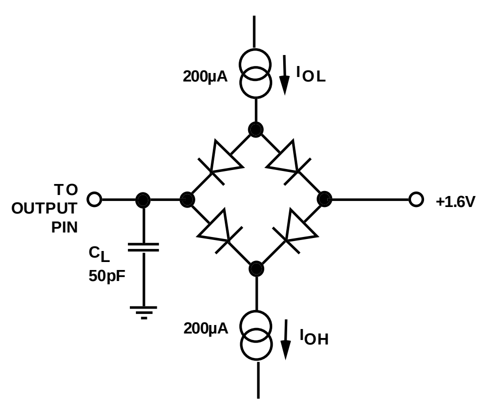


Figure 1. Load Circuit for Digital Output Timing Specifications

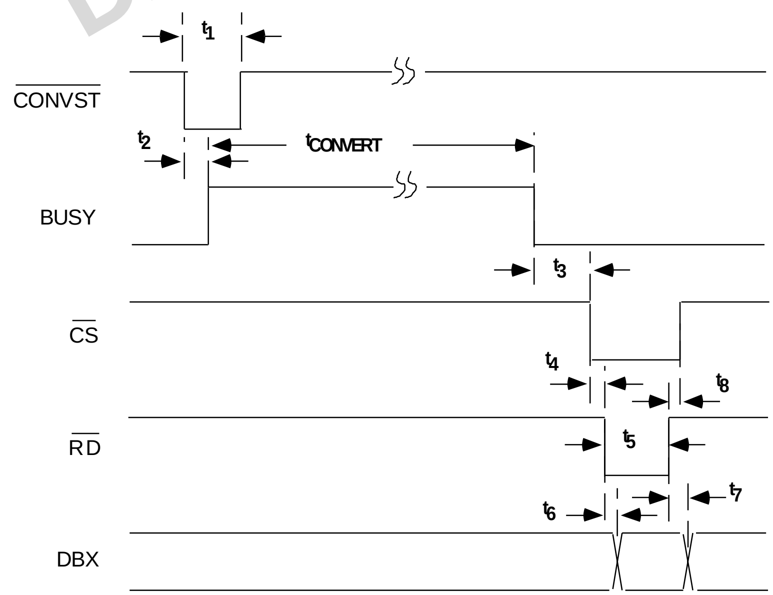


Figure 2. AD7470/AD7472 Timing Diagram

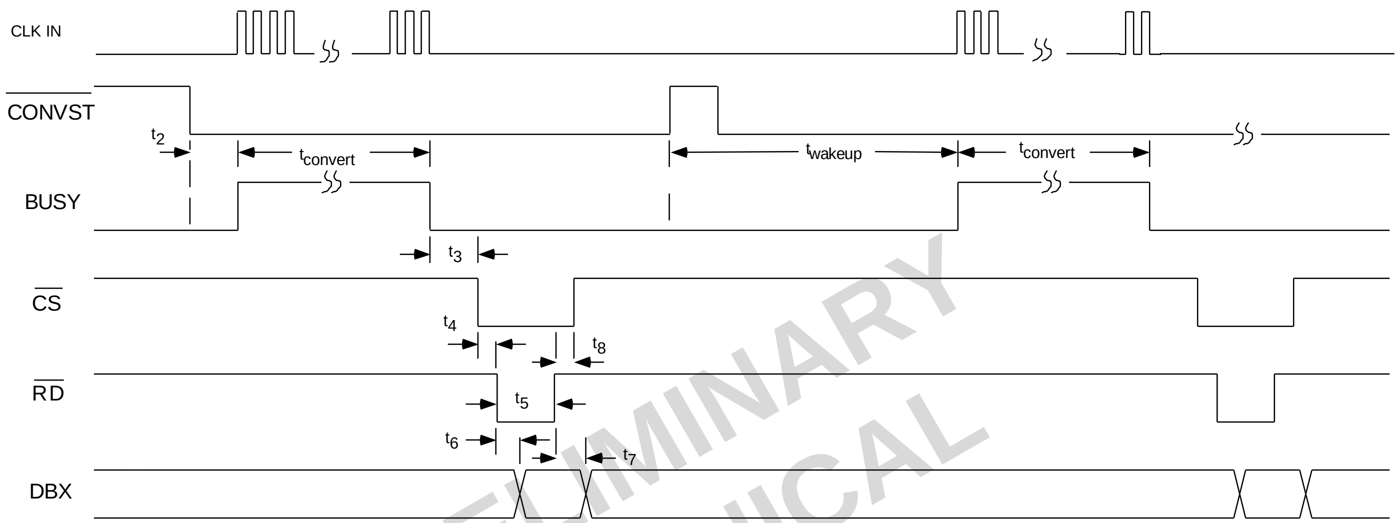


Figure 3. AD7470/AD7472 Wake-Up Timing Diagram (Burst Clock)

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND/DGND .... -0.3V to +7V
DV_{DD} to AGND/DGND .... -0.3V to +7V
V_{DRIVE} to AGND/DGND .... -0.3V to +7V
AV_{DD} to DV_{DD} .... -0.3V to +0.3V
V_{DRIVE} to DV_{DD} .... -0.3V to +0.3V
AGND TO DGND .... -0.3V to +0.3V
Analog Input Voltage to AGND .... -0.3V to AVDD+0.3V
Digital Input Voltage to DGND .... -0.3V to DVDD+0.3V
REF IN to AGND .... -0.3V to AVDD+0.3V
Input Current to Any Pin Except Supplies[2] .... ±10mA
Operating Temperature Range
Commercial (A Version) .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +150°C
SOIC, TSSOP Package Dissipation .... +450mW
θ_{JA} Thermal Impedance ... 75°C/W (SOIC) 115°C/W (TSSOP)
θ_{JC} Thermal Impedance ..... 25°C/W (SOIC) 35°C/W (TSSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs) .... +215°C
Infared (15 secs) .... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

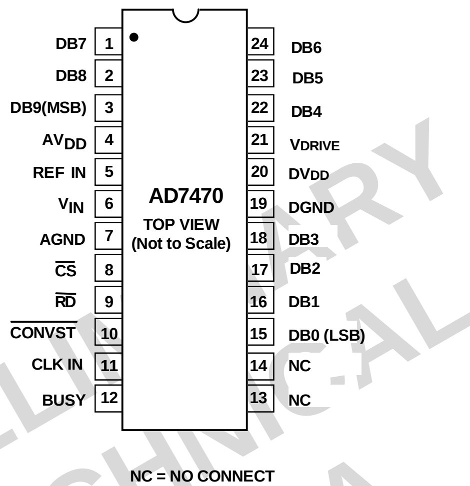
ORDERING GUIDE

Model	Range	Resolution (Bits)	Package Option[1]	Branding
AD7470ARU	-40°C to +85°C	10	RU-24	
AD7472AR	-40°C to +85°C	12	R-24	
AD7472ARU	-40°C to +85°C	12	RU-24	
EVAL-AD7470CB[2]	Evaluation Board			
EVAL-AD7472CB[2]	Evaluation Board			
EVAL-CONTROL BOARD[3]	Controller Board			

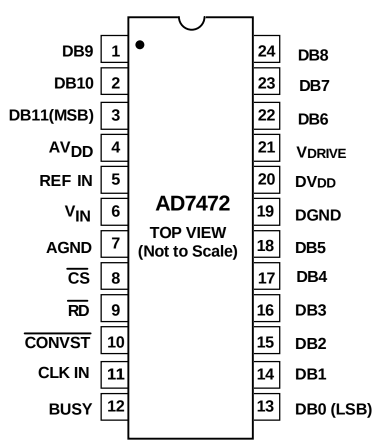
NOTES
[1]R = SOIC; RU = TSSOP.
[2]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the XX0000 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7470 PIN CONFIGURATION



AD7472 PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{CS}$ can be hardwired permantly low.
$\overline{RD}$	Read Input. Logic Input used in conjunction with $\overline{CS}$ to access the conversion result.The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to same AND gate on the input so the signals are interchangeable. $\overline{CS}$ and $\overline{RD}$ can be hardwired permanently low in which case, the data bus is always active and the result of the new conversion are clocked out subsequent to the BUSY line going low.
$\overline{CONVST}$	Conversion Start Input. Logic Input used to initiate conversion. The input track/hold amplifier goes from track mode to hold mode on the falling edge of $\overline{CONVST}$ and the conversion process is initi ated at this point. The conversion input can be as narrow as 15ns. If the $\overline{CONVST}$ input is kept low for the duration of conversion and is still low at the end of conversion, the part will automatically enter a shutdown mode. If the part enters this shutdown mode, the next rising edge of $\overline{CONVST}$ wakes the part up. Wake-up time for the part is typically 1μs.
CLK IN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7472 takes 14 full clock cycles while conversion time for the AD7470 takes 12 full clock cycles. The frequency of this master clock input therefore determines the conversion time and achievable throughput rate. The frequency range for this clock input is from 1kHz to 28MHz.
BUSY	BUSY Output. Logic Output indicating the status of the conversion process. The BUSY signal goes high from the falling edge of $\overline{CONVST}$ and stays high for the duration of conversion. Once conversion is complete and the conversion result is in the output register, the BUSY line returns low. The track/hold returns to track mode prior to the falling edge of BUSY and the acquisition time for the part begins at this point. If the $\overline{CONVST}$ input is still low when BUSY goes low, the part automatically enters its shutdown mode on the falling edge of BUSY.
REF IN	Reference Input. An external reference must be applied to this input. The voltage range for the external reference is 2.5V ±1% for specified performance.
AV_{DD}	Analog Supply Voltage, +2.7V to +5.25V. This is the only supply voltage for all analog circuitry on the AD7470/72. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to AGND.
DV_{DD}	Digital Supply Voltage, +2.7V to +5.25V. This is the supply voltage for all digital circuitry on the AD7470/72 apart from the output drivers. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to DGND.
AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7470/72. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis.
DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7470/AD7472. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0V to REFIN. The analog input presents a high dc input impedance.
V_{DRIVE}	Supply Voltage for the Output Drivers, +2.7V to +5.25V. This voltage determines the output high voltage for the data output pins. It allows the AVDD and DVDD to operate at 5V (and maximize the input signal if required) while the digital outputs can interface to 3V logic.
DB0-DB9/11	Data Bit 0 to Data Bit 9 (AD7470) and DB11 (AD7472). Parallel digital outputs which provide the conversion result for the part. These are three-state outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. The output high voltage level for these outputs is determined by the V_{DRIVE} input.

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Gain Error

The last transition should occur at the analog value 1 1/2 LSB below the nominal full scale. The first transition is a 1/2 LSB above the low end of the scale (zero in the case of AD7470/74). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions.

Track/Hold Acquisition Time

The track/hold amplifier returns into track mode after the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter is 62dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7470/72, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7470/72 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

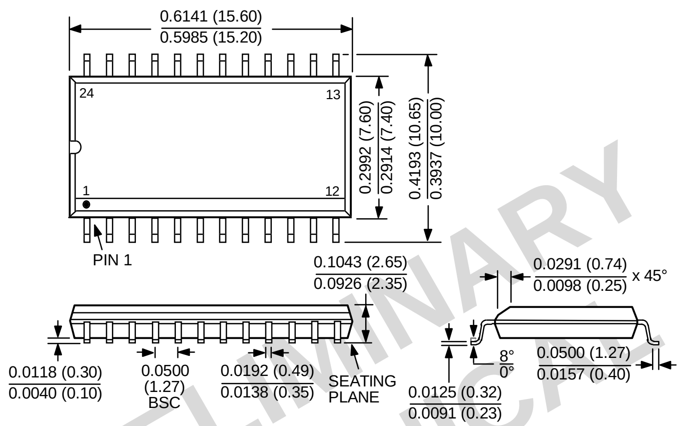
PSR (Power Supply Rejection)

Variations in power supply will affect the full-scale transition, but not the conveter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

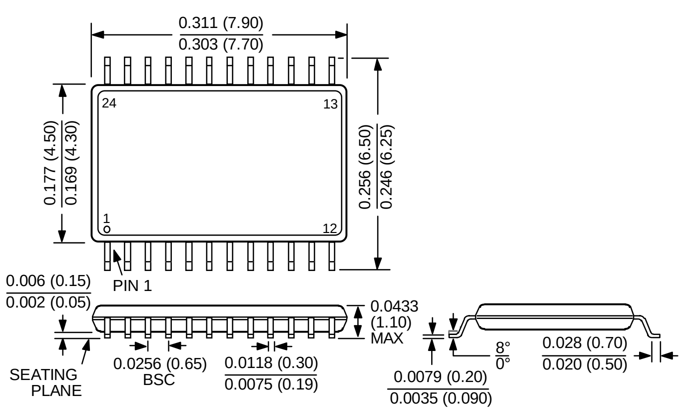
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-LEAD SOIC (R-24)



24-LEAD TSSOP (RU-24)



ADENDUM

Samples whose brand include the date code “9830” and “9838” on line 2, have an identified metastability problem which results in one conversion in approx. 1.2million giving an incorrect result.

This problem has been corrected on subsequent parts.